UD info Corp.

Industrial USB FLASH DISK
UFC-RLUH Series
Product DataSheet

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Revision History

Revision	Draft Date	History	Author
1.0	2025/9/17	New Release	Migo.Huang

Product Overview

- **Capacity**
    - BiCS5 TLC: 64GB-512GB
    - BiCS5 pSLC: 16GB-128GB
- **USB Interface**
    - SuperSpeed up to 5Gbit/s for USB 3.2 Gen 1
    - High speed up to 480Mbits/s for USB 2.0
    - Full speed up to 12Mbits/s for USB 1.1
- **Flash Interface**
    - Flash Type: 3D BiCS5
- **Performance** Note2
    - BiCS5 TLC R/W up to 220 / 100 MB/s
    - BiCS5 pSLC R/W up to 220 / 120 MB/s
- **Power Consumption**Note1
    - Active mode (Max): 230 mA
    - Idle mode: 60 mA
- **Advanced Flash Management**
    - Bad Block Management
    - SMART
    - ECC
    - Wear Leveling
- **Low Power Management**
- **Temperature Range**
    - Operation (Standard): 0°C ~ 70°C
    - Operation (Wide): -40°C ~ 85°C
    - Storage: -40°C ~ 85°C

Notes:

1. Please see Power Consumption” for details.
2. The performance is obtained from CrystalDiskMark.

1. INTRODUCTION

1.1. General Description

UDinfo UFC-UH Series is a new USB flash drive with Type-C connector applied for industry. It is compatible with the latest USB specification – USB 3.2 Gen1 Super Speed, with a maximum transfer rate of 5 Gb/s. The connector is backward compatible with USB 2.0 and USB 1.1 interfaces. With compliance with USB 3.2 specification, this USB drive can deliver up to 250 MB/s outstanding performance and operate at minimal power consumption

1.2. Flash management

1.2.1 Error Correction Code (ECC)

Flash memory cells will deteriorate with use and might generate random bit errors in the stored data. The Industrial UFC Drive applies the LDPCECC algorithm, which can detect and correct errors occurred during read process, to ensure data been read correctly, as well as protect data from corruption.

1.2.2 Wear Leveling

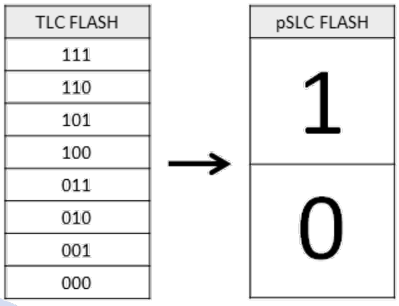
NAND flash devices can only undergo a limited number of program/erase cycles, and in most cases, the flash media are not sued evenly. If some area get updated more frequently than others, The lifetime of the device would be reduced significantly. Thus, wear leveling technique is applied to extend the lifespan of NAND flash by evenly distributing write and erase cycles across the media. UDinfo provides advanced wear leveling algorithm, which can efficiently spread out the flash usage through the whole flash media area. Moreover, by implementing both dynamic and static wear leveling algorithms, the life expectancy of the NAND flash is greatly improved.

1.2.3 Bad Block Management

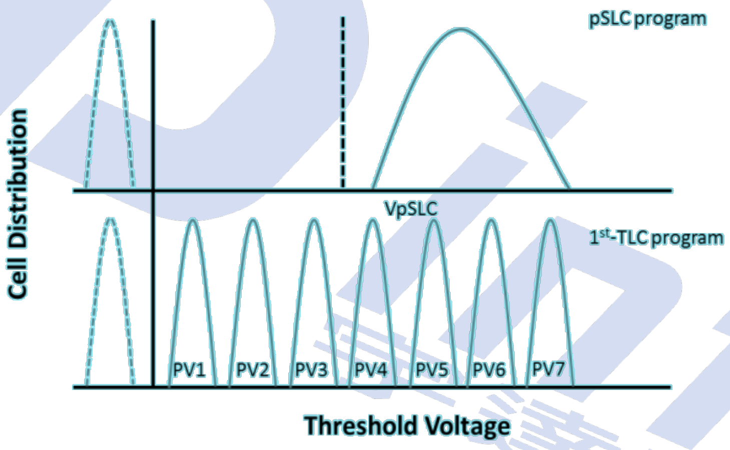
Bad blocks are blocks that include one or more invalid bits, and their reliability is not guaranteed. Blocks that are identified and marked as bad by the manufacturer are referred to as “initial bad blocks”. Bad blocks that are developed during the lifespan of the flash are named “later bad blocks”. UDinfo implements an efficient bad block management algorithm to detect the factory-produced bad blocks and manages any bad blocks that appear with use. The practice further prevents data being stored into bad blocks and improves the data reliability.

1.2.4 Pseudo SLC

Pseudo SLC (pSLC), a part of the 3D-TLC family has been proved to provide better performance and greater endurance by programming two level of the cell of 3D-TLC.The pSLC mode for 3D TLC only separates the threshold voltage to two parts and operated it to as 1-bit cell. This kind of operation for 3D TLC can speed up the programming time and extend the endurance for single cell. Differentiating the number of charges inside the floating gate becomes easier, since a more separate cell distribution reduces the chance to misjudge the threshold voltage for each cell. Additionally, endurance of pSLC is at least ten times greater than that of MLC and 3D-TLC. We believe that pSLC is the most economical alternative for NAND flash application.

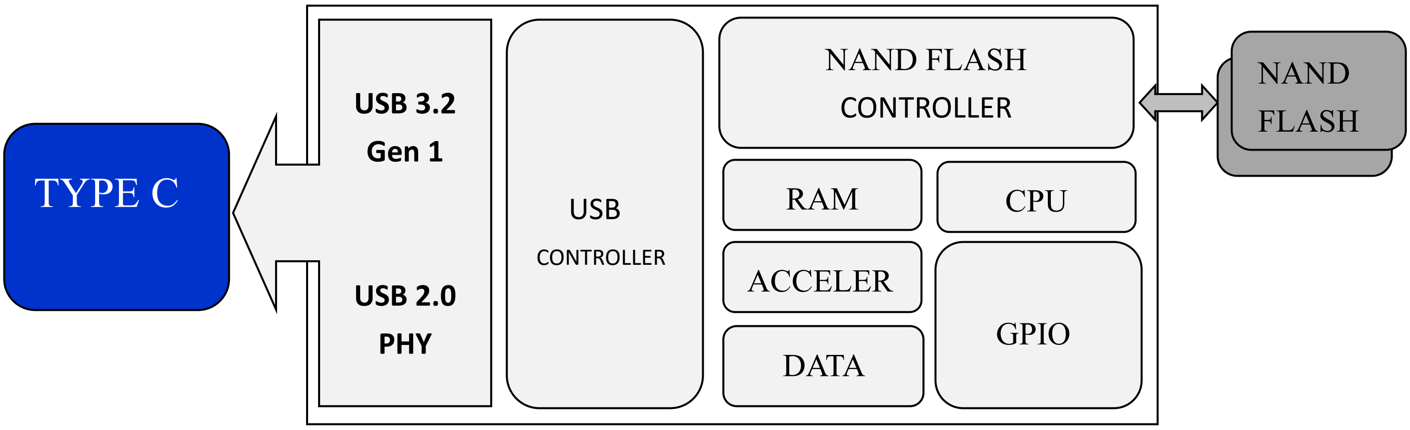


Cell Content for 3D TLC (Left) and pSLC (Right)



Cell Distribution vs. Threshold Voltage for 3D pSLC

1.3. Block Diagram



2. PRODUCT SPECIFICATIONS

- Compatible with USB specification revision 3.2 gen 1 and backward compatible with USB 3.1 gen 1, USB2.0 & USB 1.1.
- **Capacity available**
  - BiCS5 TLC: 64GB-512GB
  - BiCS5 pSLC: 16GB-128GB
- **Operation temp.**
  - Standard: 0°C ~ 70°C
  - Wide: -40°C ~ 85°C
- **Storage temp.**
  - -40°C ~ 85°C
- Compliant with USB Specification Revision 1.1 / 2.0 / 3.0
- Support Windows XP and later version
- Supports macOS® 10.8 and later
- Supports Linux® Kernel 2.4.10 and later
- No external power is required - DC 4.5V ~ 5.5V from USB port.
- **Transfer rate for USB interface**
  - Super Speed up to 5Gbit/sec for USB 3.2 GEN 1
  - High speed up to 480Mbits/sec for USB 2.0
  - Full speed up to 12Mbits/sec for USB 1.1
- **Performance**

Flash Type	Capacity	Performance (MB/s) Crystal Disk Win10	
		Read	Write
BiCS5 TLC	64GB	200	40
	128GB	220	100
	256GB	220	100
	512GB	220	100
BiCS5 pSLC	16GB	210	60
	32GB	210	60
	64GB	210	120
	128GB	210	120

Note: Sequential read/write performance is measured using CrystalDiskMark with a 1,000MB test file under a Windows environment.

3. ENVIRONMENTAL SPECIFICATIONS

3.1. Environmental Conditions

3.1.1. Temperature and Humidity

- Temperature:
  - Storage: -40°C to 85°C
  - Operational (Standard grade): 0°C to 70°C
  - Operational (Wide grade): -40°C to 85°C

- Humidity:
  - Standard grade: RH 90% under 40°C (operational)
  - Wide grade: RH 95% under 55°C (operational)

➢ **High Temperature Test Condition**

	Temperature	Humidity	Test Time
Operation (Standard)	70°C	0% RH	72 hours
Operation (Wide)	85°C	0% RH	72 hours
Storage (Standard)	85°C	0% RH	72 hours
Storage (Wide)	85°C	0% RH	168 hours

Result: No any abnormality is detected.

➢ **Low Temperature Test Condition**

	Temperature	Humidity	Test Time
Operation (Standard)	0°C	0% RH	72 hours
Operation (Wide)	-40°C	0% RH	72 hours
Storage (Standard)	-40°C	0% RH	72 hours
Storage (Wide)	-40°C	0% RH	168 hours

Result: No any abnormality is detected.

➢ **High Humidity Test Condition**

	Temperature	Humidity	Test Time
Operation (Standard)	40°C	93% RH	24 hours
Operation (Wide)	55°C	95% RH	72 hours
Storage (Standard)	40°C	95% RH	72 hours
Storage (Wide)	55°C	95% RH	96 hours

Result: No any abnormality is detected.

- **Temperature Cycle Test**

	Temperature	Test Time	Cycle
Operation (Standard)	0°C	30 min	10 cycles
	70°C	30 min	
Operation (Wide)	-40°C	30 min	20 cycles
	85°C	30 min	
Storage (Standard)	-40°C	30 min	10 cycles
	85°C	30 min	
Storage (Wide)	-40°C	30 min	50 cycles
	85°C	30 min	

Result: No any abnormality is detected.

4. ELECTRICAL SPECIFICATIONS

4.1. Power Consumption

Samples are made of Toshiba 3D NAND Flash.

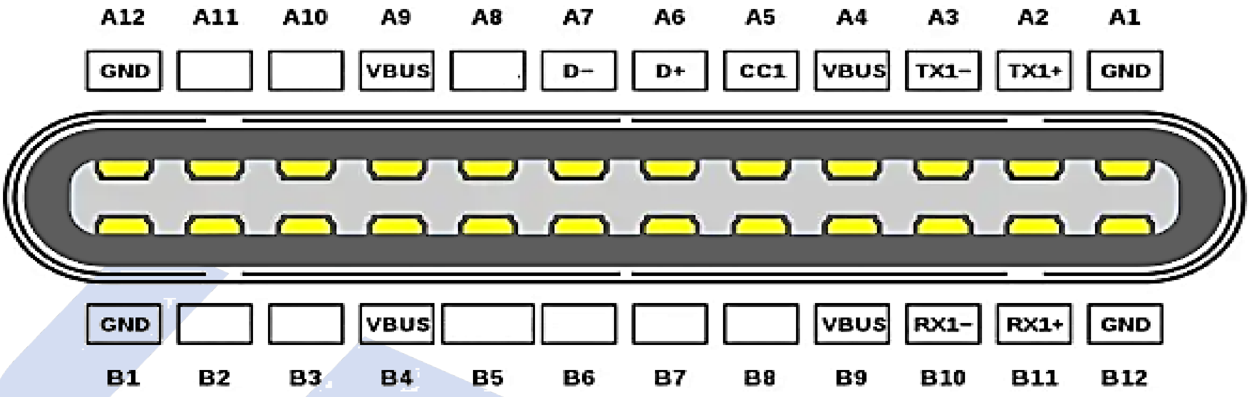
Power Consumption Max. (mA)	
Active (Max.)	230
Idle	55

4.2. Absolute Maximum Ratings

Parameter	Min.	Typ.	Max.	Unit
Operating Temperature (Standard)	0	25	70	℃
Storage Temperature (Standard)	-40	25	85	℃
Operating Temperature (Wide)	-40	25	85	℃
Storage Temperature (Wide)	-40	25	85	℃
1.1V regulator power supply	1.04	1.12	1.2	V
1.8V regulator power supply	1.76	1.86	2	V
3.3V Regulator Power Supply	3.15	3.3	3.45	V
5.0V Regulator Power Supply	3	5	5.5	V
2.5V regulator power supply	2.35	2.5	2.7	V
1.2V regulator power supply	1.13	1.2	1.3	V

5. INTERFACE

5.1. Pin Assignment and Descriptions



Pin Number	Type	Pin Number	Type	Function
A1	GND	**B12**	GND	Ground return
A2	SSTXp1 ("TX1+")	**B11**	SSRXp1 ("RX1+")	SuperSpeed differential pair
A3	SSTXn1 ("TX1-")	**B10**	SSRXn1 ("RX1-")	SuperSpeed differential pair
A4	V_{BUS}	**B9**	–	Bus Power
A5	CC1	**B8**	–	Configuration channel
A6	D+	**B7**	–	USB 2.0 differential pair
A7	D-	**B6**	–	USB 2.0 differential pair
A8	–	**B5**	–	Sideband use (SBU)
A9	V_{BUS}	**B4**	V_{BUS}	Bus Power
A10	–	**B3**	–	SuperSpeed differential pair
A11	–	**B2**	–	SuperSpeed differential pair
A12	GND	**B1**	GND	Ground return

6. DC CHARACTERS

6.1. DC characteristics of I/O Cells

symbol	Parameter	Conditions	MIN	TYP	MAX	Unit
VCCK	Core Power Supply	Core Area	0.99	1.1	1.21	V
VCC3IO	Power Supply	1.8V I/O	1.62	1.8	1.98	V
		3.3V I/O	3.0	3.3	3.6	V
Temp	Junction Temperature		0	25	115	℃
V_{IL}	Schmitt Trigger	VCC3IO = 3.3V	0.35 * VCC3IO			V
	CMOS Trigger		0.5 * VCC3IO			
	Differential		PAD_VREF			
V_{IH}	Schmitt Trigger		0.65 * VCC3IO			V
	CMOS Trigger		0.5 * VCC3IO			
	Differential		PAD_VREF			
V_{IL}	Schmitt Trigger	VCC3IO = 1.8V	0.41 * VCC3IO			V
	CMOS Trigger		0.53 * VCC3IO			
	Differential		PAD_VREF			
V_{IH}	Schmitt Trigger		0.69 * VCC3IO			V
	CMOS Trigger		0.53 * VCC3IO			
	Differential		PAD_VREF			
V_{OL}	Output Low voltage	|Iol| = 2 ~ 16 mA			0.4	V
V_{OH}	Output High voltage	|Ioh| = 2 ~ 16 mA	VCC3IO- 0.4			V
Rpu	Input Pull-Up Resistance	PU=high, PD=low		75		KΩ
Rpd	Input Pull-Down Resistance	PU=high, PD=low		75		KΩ
Iin	Input Leakage Current	Vin = VCC3I or 0			10	µA
Ioz	Tri-state Output Leakage Current		-10	±1	10	µA

7. PHYSICAL DIMENSION